IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of the claims:

1-6. (Canceled)

7. (Original) A system comprising:

a memory cell string that includes a first memory cell coupled to a second memory cell;

a sense amplifier coupled to the memory cell string and configured to:

detect a first voltage at a node between the first and second memory cells at a first time;

detect a second voltage at the node at a second time subsequent to a write sense current being applied across the first memory cell;

compare the first and second voltages; and

cause a logic level associated with the first memory cell to be stored in response to comparing the first and second voltages.

8. (Original) The system of claim 7 further comprising:

a voltage source coupled to a first end of the memory cell string in response to the first end being closest to the first memory cell; and

a ground source coupled to a second end of the memory cell string that is opposite the first end of the memory cell string.

9. (Original) The system of claim 8 further comprising:

a first bit line coupled to the sense amplifier and configured to provide the first and second voltages to the sense amplifier, and a second bit line for writing the first and second memory cells.

10. (Original) The system of claim 9 further comprising:

a transistor configured to cause the first and second voltages to be provided on the first bit line.

11. (Original) The system of claim 10 wherein the transistor comprises a voltage follower transistor.

12. (Original) The system of claim 10 wherein the transistor includes a gate connection, a source connection, and a drain connection, wherein the gate connection is coupled to the node, wherein the source connection is coupled to the first bit line, and where in the drain connection is coupled to a voltage source.

13. (Original) The system of claim 9 wherein the sense amplifier includes a first differential amplifier coupled to the first bit line, a switch coupled to the first differential amplifier, and a capacitor coupled to the switch, and wherein the first differential amplifier is configured to cause the first voltage to be stored on the capacitor in response to the switch being closed.

14. (Original) The system of claim 13 wherein the sense amplifier includes a current source coupled to the first bit line.

15. (Original) The system of claim 13 wherein the sense amplifier includes a resistor coupled to the first bit line.

16. (Original) The system of claim 13 wherein the sense amplifier includes a second differential amplifier, and wherein the second differential amplifier is configured to compare the first voltage to the second voltage in response to the switch being open.

17. (Original) The system of claim 16 further comprising:

a register configured to store the logic level in response to a signal from the second differential amplifier.

18. (Original) A method of performing a read operation from a first memory cell comprising:

providing a first voltage source to a memory cell string that includes a first memory cell coupled to a second memory cell;

providing a ground source to the memory cell string;

providing a second voltage source to a transistor coupled to a node between the first memory cell and the second memory cell and coupled to a bit line that is configured to write the first memory cell in conjunction with a word line; and

determining whether a voltage change occurred at the node in response to applying a first write sense current across the first memory cell using the word line.

19. (Original) The method of claim 18 further comprising:

storing a logic level associated with a first state in response to determining that the voltage change occurred.

20. (Original) The method of claim 19 further comprising:

storing a logic level associated with a second state in response to determining that the voltage change did not occur.

21. (Original) The method of claim 18 further comprising:

determining whether the voltage change occurred at the node in response to applying the first write sense current across the first memory cell using the word line and applying a second write current across the first memory cell using the bit line.